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[54] **DELAY CIRCUIT AND METHOD**

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[*] Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

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Related U.S. Application Data

[63] Continuation of application No. 08/595,512, Feb. 1, 1996, abandoned, which is a continuation of application No. 08/411,556, Mar. 28, 1995, abandoned, which is a continuation-in-part of application No. 08/365,685, Dec. 29, 1994.

[51] **Int. Cl.**[6] **H03K 5/13**

[52] **U.S. Cl.** **327/285**; 327/288; 327/263; 327/278

[58] **Field of Search** 327/285, 276, 327/277, 278, 284, 281, 288, 263, 264; 365/194; 331/57

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[57] **ABSTRACT**

A reduced area delay circuit and method are disclosed. The delay circuit uses a constant current source and a constant current drain to charge and discharge a capacitor and thus control the delay time of the delay circuit. The constant current source and drain can be implemented using current mirrors formed by configuring MOSFET transistors in a common source configuration. The delay circuit method includes the steps of receiving an input signal, delaying the input signal by using a constant current source or drain in combination with a capacitor, and then buffering the voltage on the capacitor using two inverters. A programmable delay circuit is also disclosed by adding additional pairs of current mirrors to the delay circuit and selectively enabling the pairs to adjust the delay time.

15 Claims, 2 Drawing Sheets